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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,746	09/12/2003	Chia-Ta Hsieh	TS02-353	8142

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EXAMINER

CHEN, ERIC BRICE

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/661,746

Applicant(s)

HSIEH, CHIA-TA

Examiner

Eric B. Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-15 is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☒ Claim(s) 8 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/24/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election without traverse of claims 1-15 in the reply filed on July 5, 2005 is acknowledged.

***Priority***

2. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

***Specification***

3. Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsieh et al. (U.S. Patent No. 6,441,429) ("Hsieh I")

6. As to claim 1, Hsieh discloses a method to form MOS gates in an integrated circuit device (column 1, lines 45-48) comprising: forming a dielectric layer (14) overlying a substrate (11) (column 5, lines 37-40; Figure 3B); forming a polysilicon layer (15) overlying said dielectric layer (14) (column 5, lines 41-44); forming a silicon oxide layer (16) overlying said polysilicon layer (15) (column 5, lines 44-48); forming a patterned masking layer (17') overlying and selectively exposing said silicon oxide layer (column 5, lines 60-67; column 6, lines 1-7); thereafter oxidizing said polysilicon layer (15) to increase thickness of said exposed silicon oxide layer (22) wherein said thickened silicon oxide layer encroaches under the edges of said masking layer and wherein said silicon oxide layer does not thicken under other interior areas of said masking layer (column 6, lines 18-32); thereafter removing said masking layer (17M) (column 6, lines 33-37); thereafter etching said silicon oxide layer to selectively expose said polysilicon layer where said silicon oxide layer did not thicken (column 6, lines 39-47; Figure 3E); and thereafter etching through said exposed polysilicon layer to thereby form MOS gates in the manufacture of said integrated circuit device (column 6, lines 39-47; Figure 3E).

7. As to claim 2, Hsieh I discloses that said MOS gates comprise floating gates for split gate flash devices (column 6, lines 39-41).

8. As to claim 3, Hsieh I discloses that said step of forming a silicon oxide layer comprises thermal oxidation of said polysilicon layer (15) (column 5, lines 44-48).

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9. As to claim 4, Hsieh I discloses that said step of thereafter etching said silicon oxide layer (16) to selectively expose said polysilicon layer comprises an oxide dip (column 6, lines 7-10).

10. As to claim 5, Hsieh I discloses that said MOS gates (15F) have a dish-shaped cross-sectional profile (column 6, lines 29-32; Figure 3D).

11. As to claim 6, Hsieh I discloses that said masking layer (17) comprises silicon nitride (column 5, lines 61-64).

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh I in view of Hsieh et al. (U.S. Patent No. 6,159,801) ("Hsieh II").

14. As to claim 7, Hsieh I does not expressly disclose that edges of said MOS gates overlie isolation structures in said substrate. However, Hsieh II discloses a method to form MOS gates in an integrated circuit device (column 5, lines 62-67), including forming the edges of said MOS gates overlying isolation structures (130) (column 6, lines 42-45) in said substrate (Figure 3G). Hsieh II teaches that this structure increases the coupling ratio of the source to floating gate, thus preventing punch-through and junction breakdown (column 3, lines 66-67; column 4, lines 1-8). Therefore, it would

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have been obvious to one of ordinary skill in the art at the time the invention was made to form the edges of said MOS gates overlying isolation structures in said substrate. One who is skilled in the art would be motivated to increase the coupling ratio of the source to floating gate.

***Allowable Subject Matter***

15. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach or suggest removing said silicon oxide layer after said step of etching through said exposed polysilicon layer, as in the context of claim 8. The closest prior art, Hsieh I, discloses a method to form MOS gates in an integrated circuit device (column 1, lines 45-48), including thereafter oxidizing said polysilicon layer (22) to increase thickness of said exposed silicon oxide layer (column 6, lines 33-37).

Silicon layer (22) remains in the final MOS device structure (Figure 5K). However, there is no motivation or suggestion of removing said silicon oxide layer after said step of etching through said exposed polysilicon layer, as in the context of claim 8.

17. Claims 10-15 are allowed.

18. The following is an examiner's statement of reasons for allowance: the prior art fails to teach or suggest thereafter removing said silicon oxide layer, as in the context of claim 10. The closest prior art, Hsieh I, discloses a method to form MOS gates in an

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integrated circuit device (column 1, lines 45-48) including thereafter oxidizing said polysilicon layer to increase thickness of said exposed silicon oxide layer (22) (column 6, lines 33-37). Silicon layer (22) remains in the final MOS device structure (Figure 5K). However, there is no motivation or suggestion of thereafter removing said silicon oxide layer, as in the context of claim 10.

19. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al. (U.S. Patent No. 6,486,032) discloses a method of fabricating a floating gate flash memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone

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number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

July 20, 2005

EBC

NADINE G. NORTON  
SUPERVISORY PATENT EXAMINER

*Nadine*